

1004783-030402

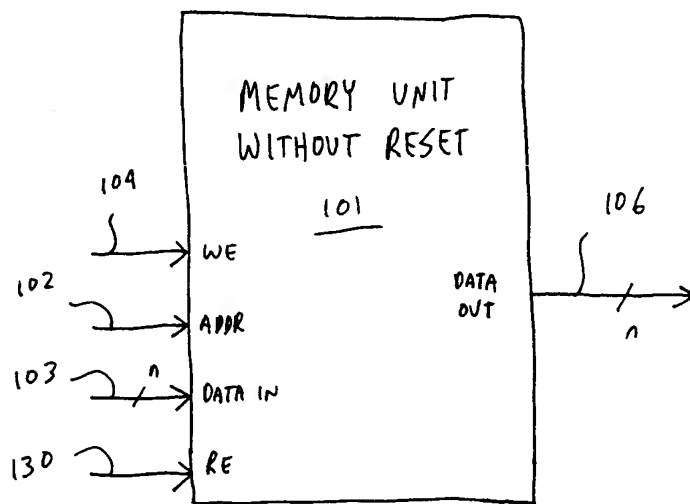


FIGURE 1

**REPORT**

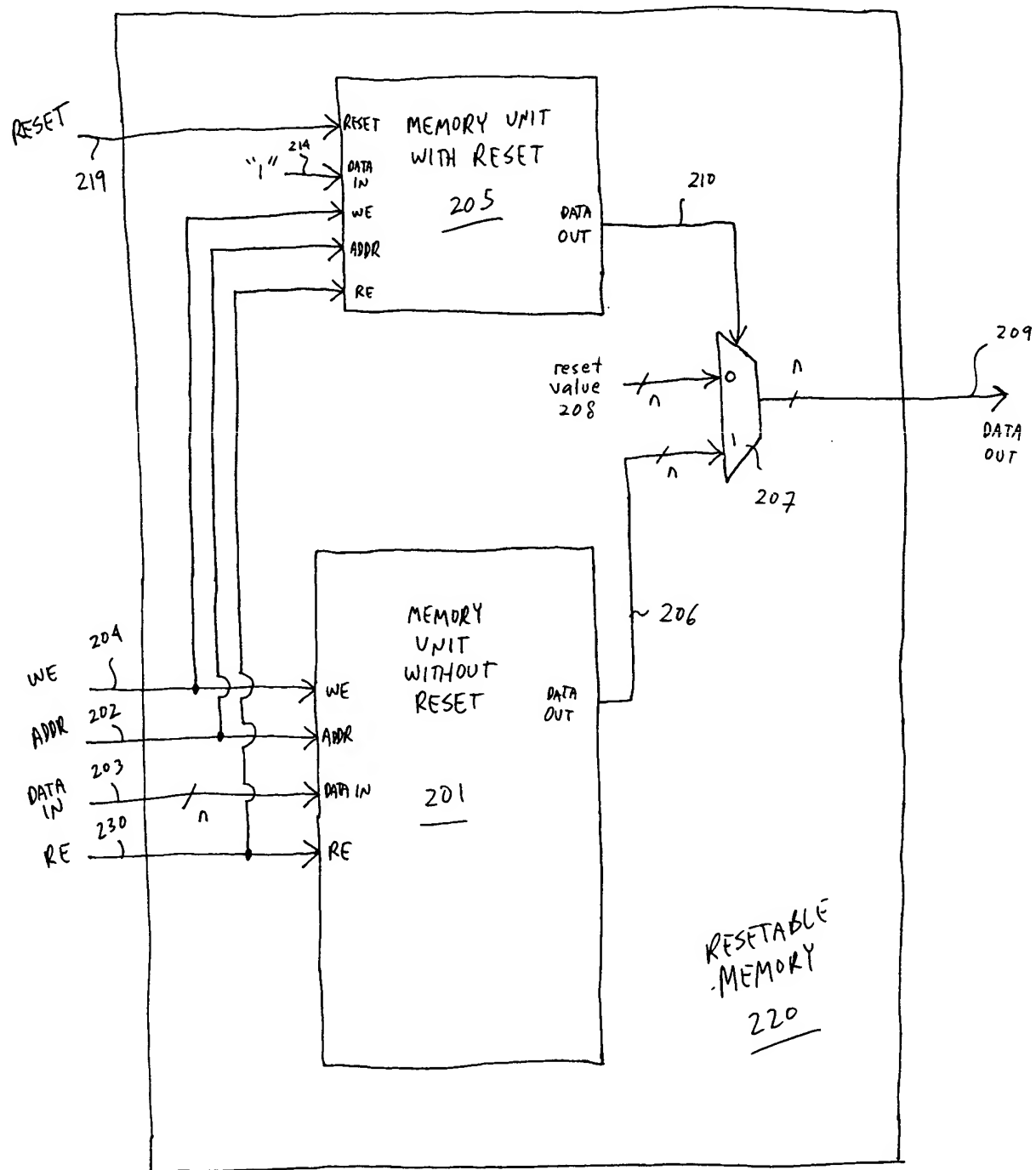


FIGURE 2A

2001-2004

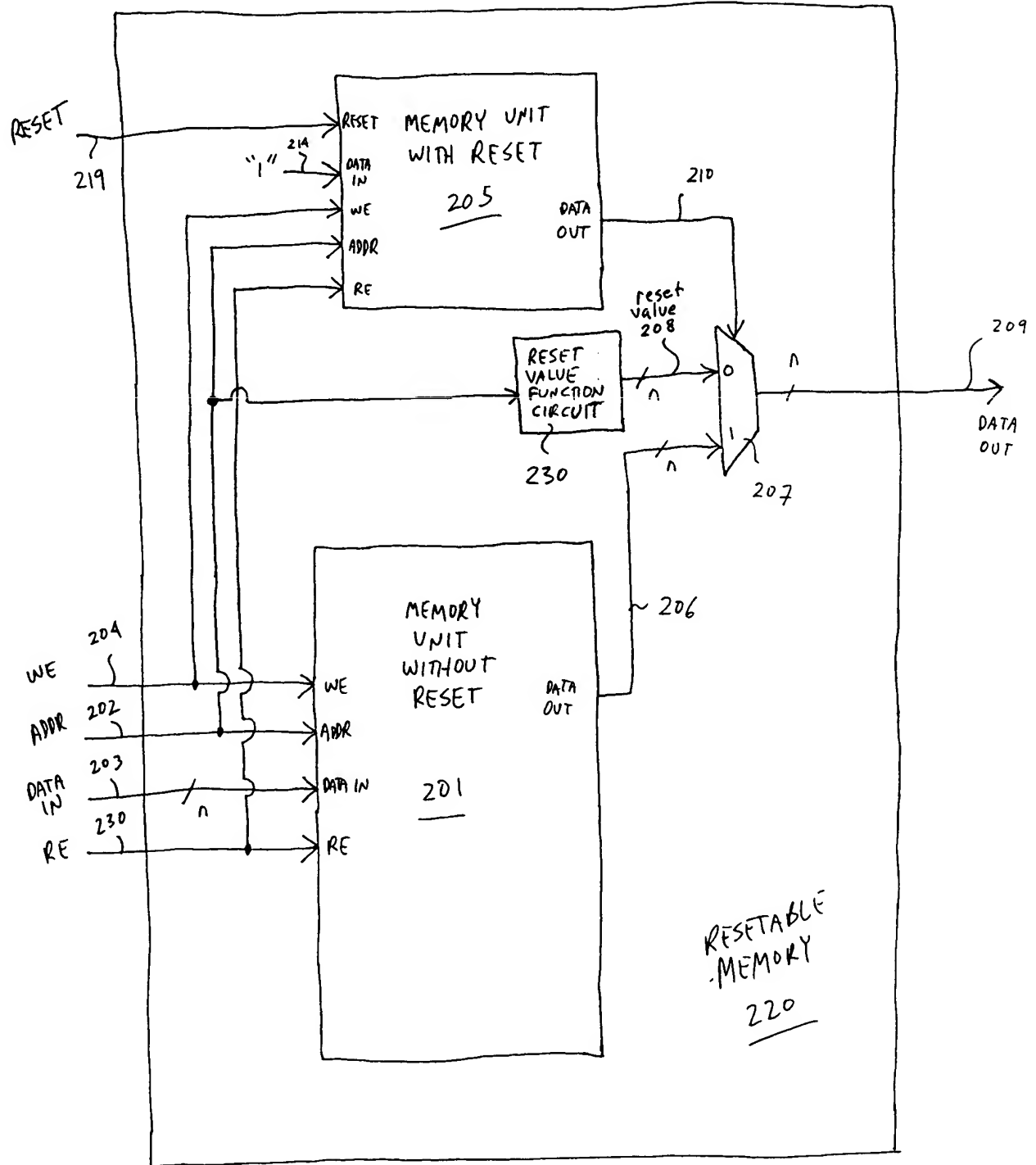


FIGURE 2B

**module** synReset(data\_in, addr, reset, we, clk, data\_out);

**parameter** data\_width = 1024;

**parameter** addr\_width = 10;

**parameter** RAMsize = 8;

**parameter** reset\_value = 8'D0;

**input** [data\_width-1:0] data\_in;

**input** [addr\_width-1:0] addr;

**input** reset, we, clk;

**output** [data\_width-1:0] data\_out;

**integer** i;

**reg** [data\_width-1:0] mem [RAMsize-1:0];

**wire** [data\_width-1:0] data\_out;

//synthesis loop\_limit 2000

**always** @(posedge clk)

**begin**

**if**(reset == 1'b1)

**begin**

**for** (i=0; i < RAMsize ; i=i+1)

**begin**

            mem[i] = reset\_value;

**end**

**end else if**(we == 1'b1)

**begin**

        mem[addr] = data\_in;

**end**

**end**

**assign** data\_out = mem[addr];

**endmodule**

FIGURE 2C

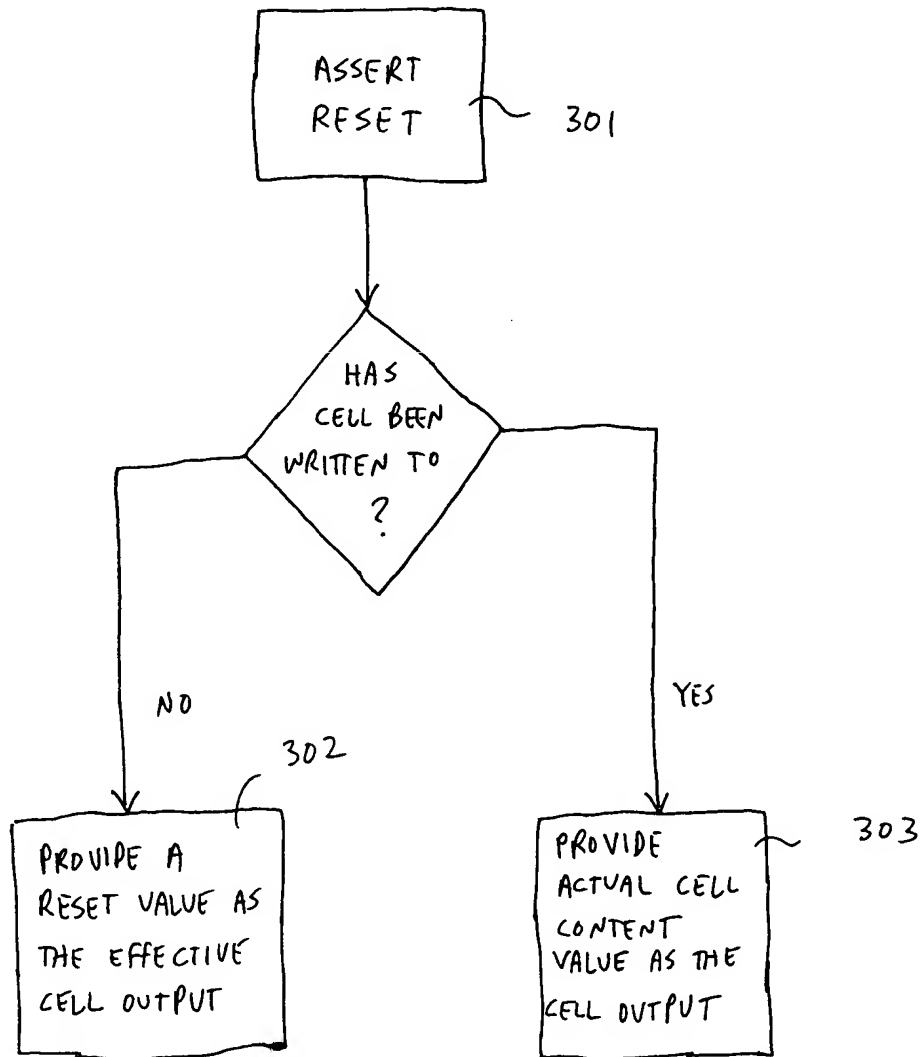


FIGURE 3

1004787-03043

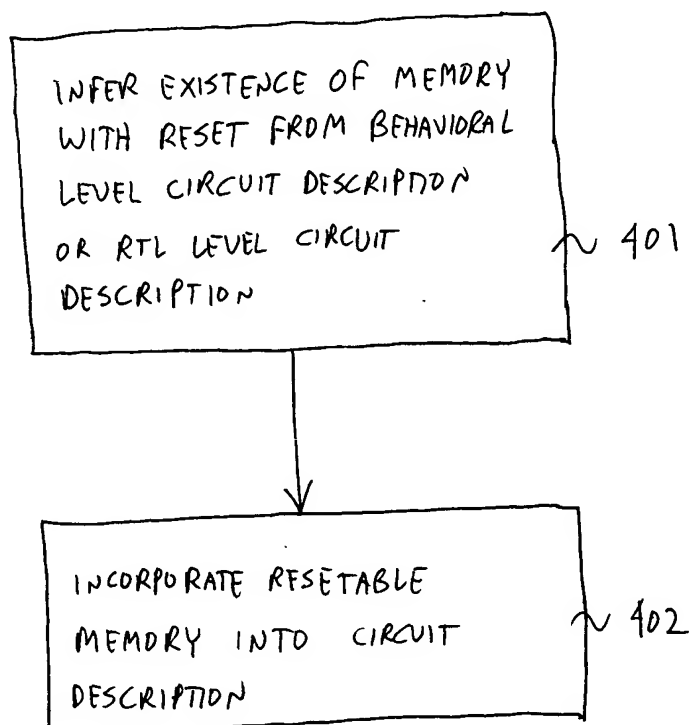


FIGURE 4

10001387-00000

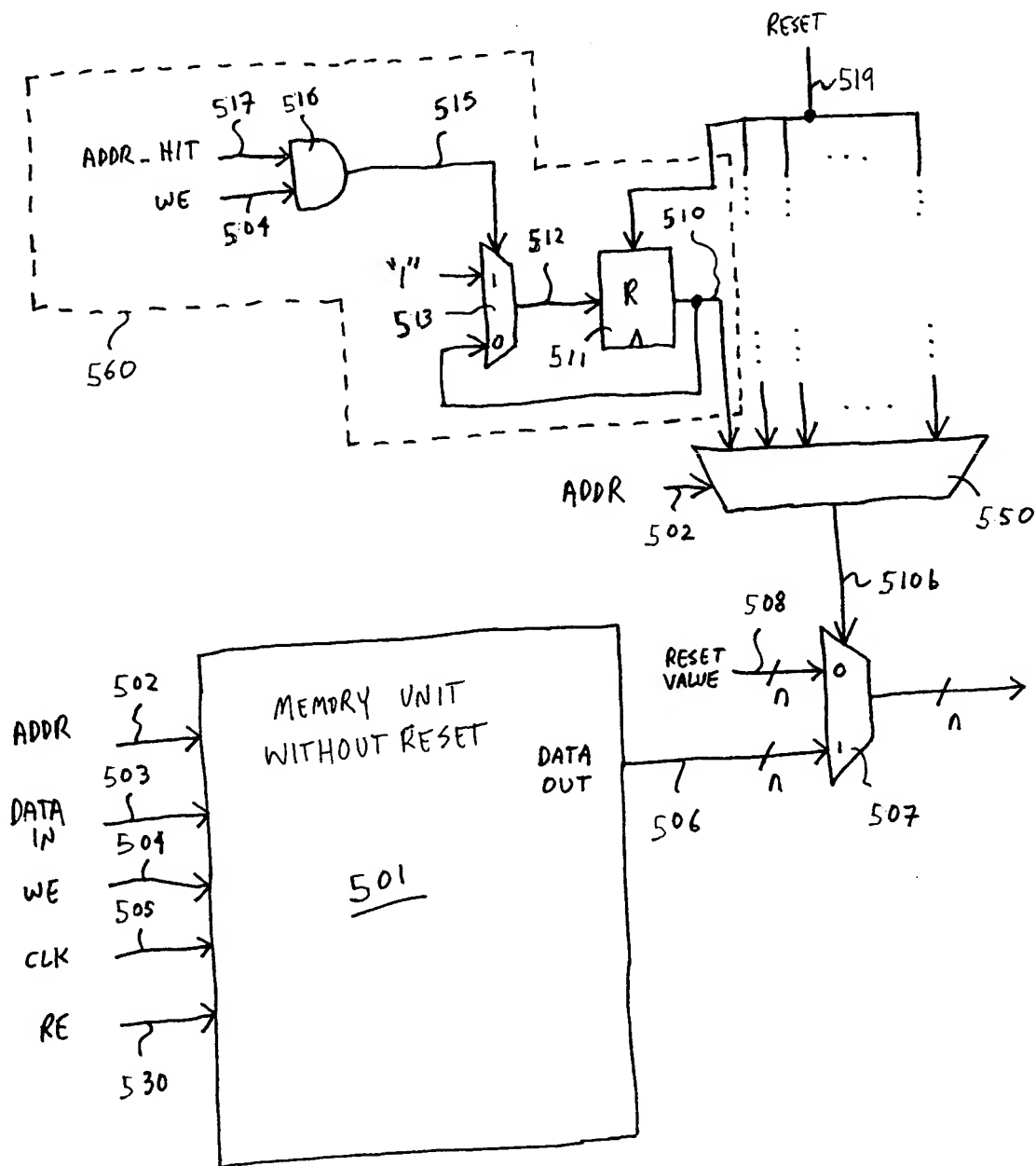


FIGURE 5.

10094787-030403

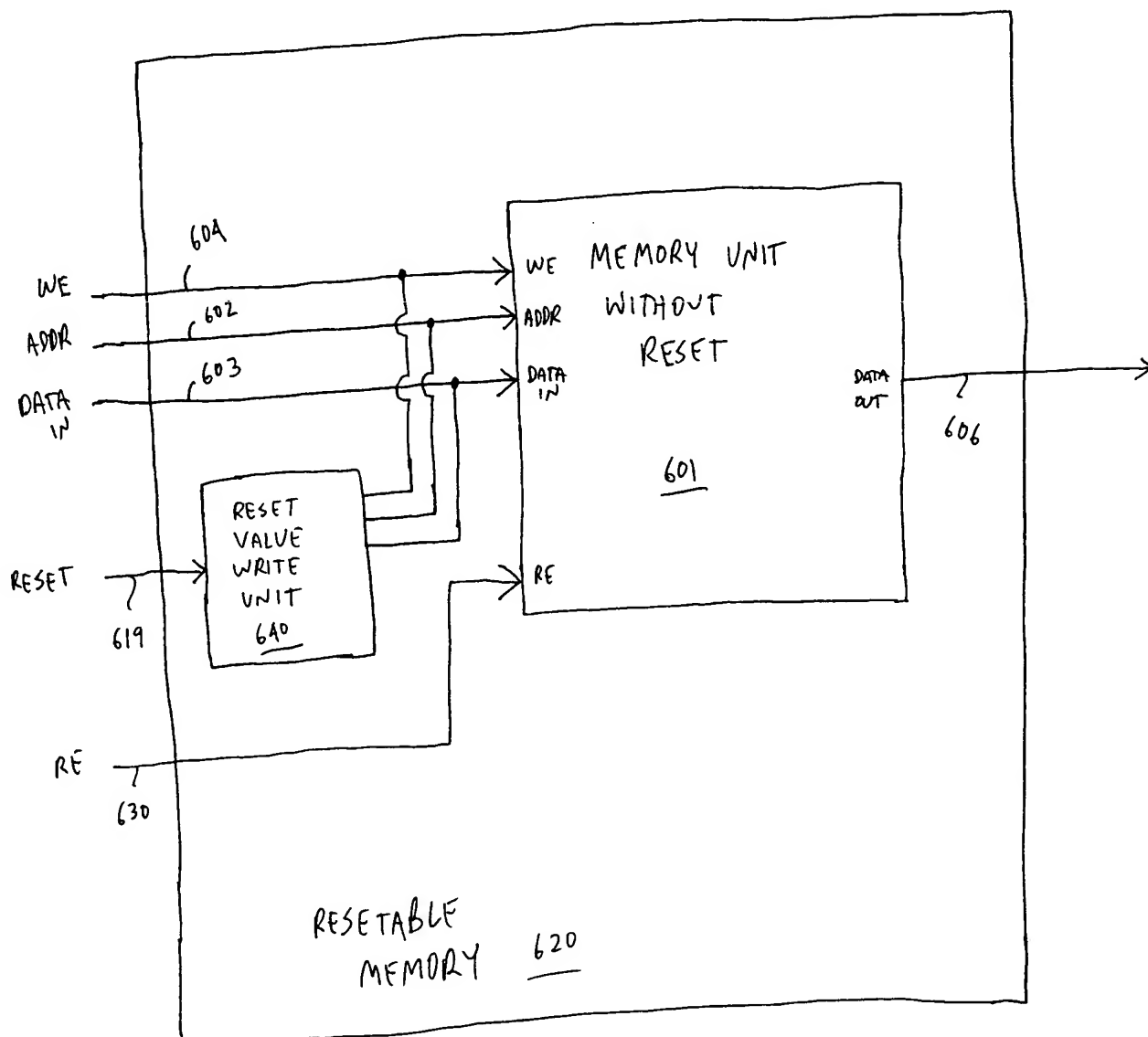


FIGURE 6

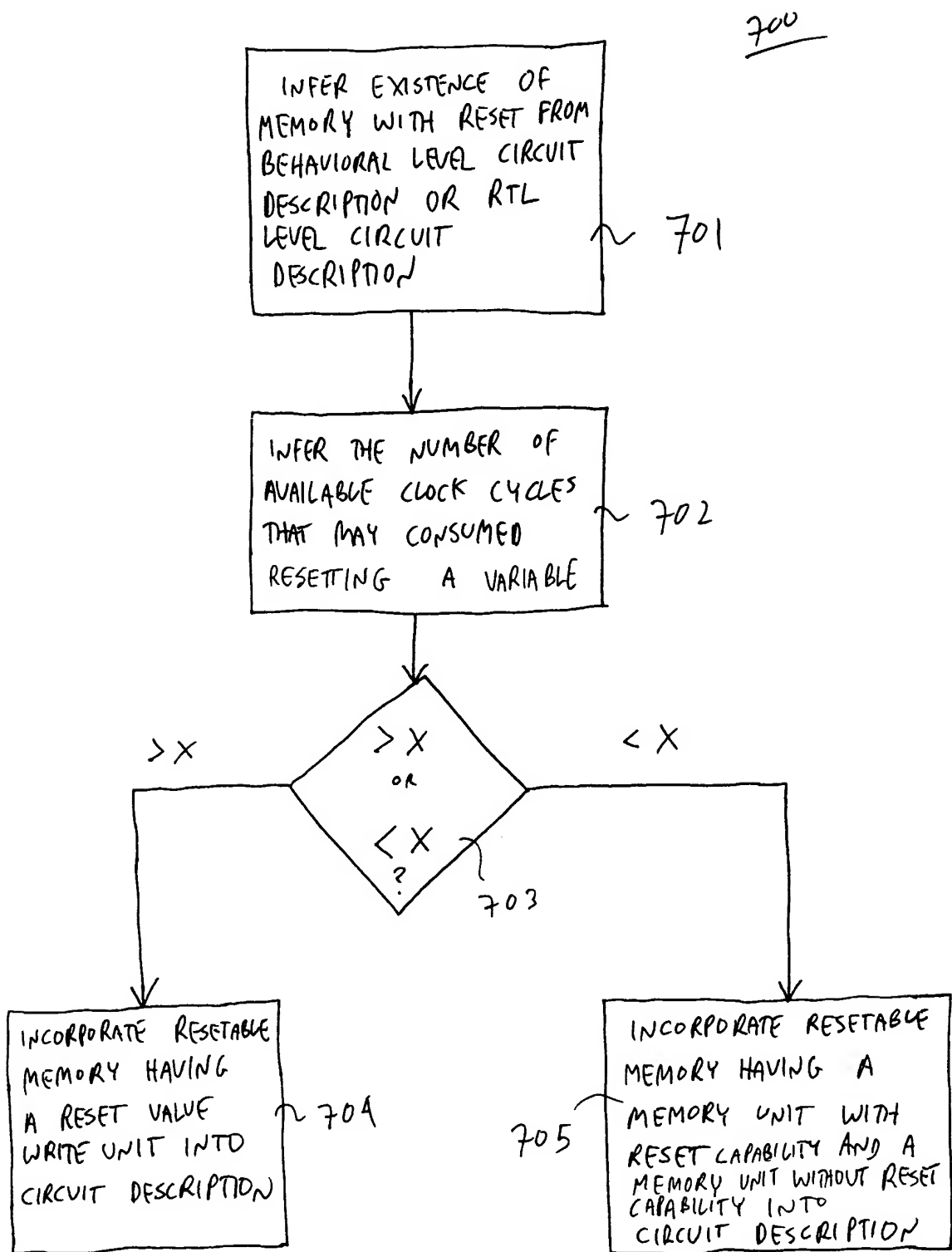


FIGURE 7

20250428 14:00:00

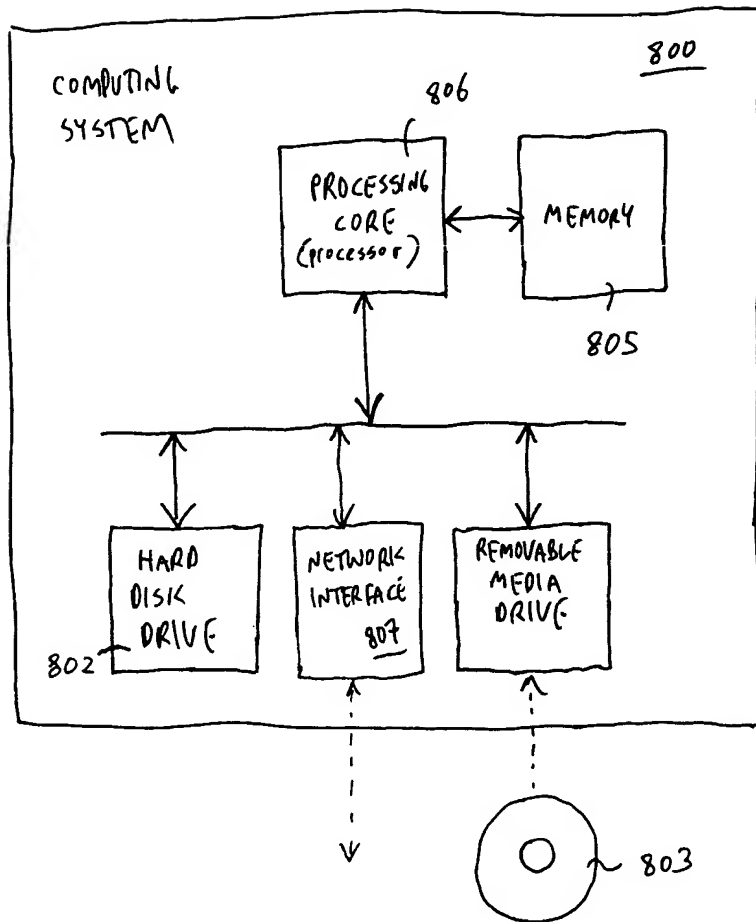


FIGURE 8